

1 rule 2
2 34. (New) The method of claim 33 wherein the first polarity is different
than the second polarity.

35. (New) A method of fabricating a transistor in an integrated circuit
device comprising:
providing a semiconductor substrate;
forming a gate oxide on the semiconductor substrate;
forming a gate on the gate oxide;
implanting a first pocket implant and a second pocket implant into the
semiconductor substrate using the gate as a mask; and
diffusing the first and second pocket implants laterally to increase a reverse
short channel effect of the transistor.

36. (New) The method of claim 35 wherein the diffusing causes the first
pocket implant to merge with the second pocket implant.

37. (New) The method of claim 35 further comprising implanting an
enhancement implant in the semiconductor implant.--

REMARKS

Applicants have amended claim 21 and 24-26, canceled claims 1-20 and added
claims 27-37. Claims 22-23 remain unchanged. Claims 21-37 are pending in this application.
Applicants respectfully request consideration and allowance of the pending claims.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this
Application are in condition for allowance. The issuance of a formal Notice of Allowance at
an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Gregory S. Bishop
Reg. No. 41,621

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (650) 326-2400 / Fax: (415) 576-0300
GSB/ka

PA 184875 v1

008290" 25290950